APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,881	07/07/2005	Wolfgang Stidl	DE03 0015 US	6245

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EXAMINER
PEARSON, DAVID J

ART UNIT	PAPER NUMBER
2437	

NOTIFICATION DATE	DELIVERY MODE
02/11/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

	Application No.	Applicant(s)
Office Action Summary	10/541,881	STIDL ET AL.
	Examiner	Art Unit	
	DAVID J. PEARSON	2437	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS,
WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>07 July 2005</u>.

2a) ☐ This action is FINAL.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
   closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-10</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-10</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>07 July 2005</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) ☒ All b) ☐ Some * c) ☐ None of:

   1. ☒ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
      application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date <u>07072005</u>.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1.   A Preliminary Amendment was filed with the instant application on 07/07/2005.

Claims 1-10 have been amended. Claims 1-10 have been examined.

Information Disclosure Statement

2.   The information disclosure statement (IDS) submitted on 07/07/2005 is in

compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure

statement is being considered by the examiner.

Claim Objections

3.   Claim 10 is objected to under 37 CFR 1.75(c) as being in improper form because

a multiple dependent claim should refer to other claims in the alternative only. See

MPEP § 608.01(n). Accordingly, the claim has been considered as best understood by

the Examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly
claiming the subject matter which the applicant regards as his invention.

4.   Claims 2 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

Regarding claim 2, the phrase "for example" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim 10 provides for the use of "at least one circuit arrangement as claimed in claim 1 and/or of the method as claimed in claim 5", but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5.   Claim 10 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 10 depends on claim 1, a system claim, and claim 5, a method claim. Claim 10 is directed towards two separate statutory classes and therefore, non-statutory subject matter.

Claim 10 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper

definition of a process, i.e., results in a claim which is not a proper process claim under

35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and

Clinical Products, Ltd. v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1-6 and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by

Force et al. (U.S. Patent 5,533,123; hereafter referred to as "Force").

For claim 1, Force teaches a microelectric circuit arrangement intended for

protecting at least one electronic component against illicit manipulation and/or

unauthorized access, having

At least one activating unit for checking that at least one activating condition is

met (note column 23, lines 19-21) and for activating at least one preventing unit that is

also associated with the circuit arrangement and that is connected to the activating unit

(note column 23, lines 21-27), by means of which preventing unit the component can be

at least partly de-activated and/or at least partly destroyed in the event of illicit

manipulation and/or unauthorized access (note column 25, lines 14-34).

For claim 5, Force teaches a method of protecting at least one electronic component against illicit manipulation and/or unauthorized access, characterized by the following method steps:

Checking that at least one activating condition is met by means of at least one activating unit (note column 23, lines 19-21),

In the event of illicit manipulation of the component and/or unauthorized access to the component activating at least one preventing unit that is connected to the activating unit (note column 23, lines 21-27) and

At least partly de-activating the operation of the component and/or at least partly destroying the component, by means of the preventing unit (note column 25, lines 14-34).

For claim 10, Force teaches the use of at least one circuit arrangement as claimed in claim 1 and/or of the method as claimed in claim 5 for the self-destruction of at least one integrated circuit in the event of unauthorized use in the field or of an illicit attempt to analyze the integrated circuit by at least partial reverse preparation (note column 23, lines 19-72 and column 25, lines 14-34).

For claim 2, Force teaches claim 1, characterized in that the preventing unit is constructed

In analog circuit technology or

In at least directly digital circuit technology, in the form of for example at least one fuse and/or at least one antifuse (note column 26, lines 16-20).

For claims 3 and 8, Force teaches claims 1 and 5, characterized in that the activating unit is arranged

To recognize once or more than once at least one illicit command (note column 22, lines 15-18),

To recognize a multiplicity of difference illicit operations (note column 23, lines 46-52)

To issue at least one specific activating command (note column 25, lines 14-21)

To issue at least one activating command together with data that addresses a plurality of components by means of at least one group coding, or an individually coded component (note column 26, lines 45-67), and/or

To recognize once or more than once at least one physical attack on the component, by means of sensor circuitry belonging to the component that is intended for this purpose (note column 15, lines 42 and 64; column 16, line 13; column 17, line 36; column 18, line 51; column 19, line 55; column 21, line 28).

For claims 4 and 9, Force teaches claims 1 and 5, characterized in that the preventing unit is arranged

To prevent an internal oscillator form beginning to oscillate

To prevent an oscillator for an external clock signal from beginning to oscillate,

To switch off a high-voltage limiter, in particular by means of permanent programming,

To prevent the build-up of a high voltage,

To reprogram the allocation of addresses and/or the allocation of data,

To load the memory element of the component with illicit values of data (note column 26, lines 16-21), and/or

To switch on an increased current drain in the operating state of the quiescent state.

For claim 6, Force teaches claim 5, characterized in the check on whether the activating condition is met is made

By analyzing at least one data stream applied from outside (note column 22, lines 15-18) or

By signals from the internal sensor circuitry of the component (note column 15, lines 42 and 64; column 16, line 13; column 17, line 36; column 18, line 51; column 19, line 55; column 21, line 28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Force as

applied to claims 5 and 6 above, and further in view of Beuten et al. (U.S. Patent

Application Publication 2003/0018902; hereafter referred to as "Beuten").

For claim 7, Force differs from the claimed invention in that they fail to teach:

If the activation condition is met, recognition of this fact and the desired effects it

is to have are placed in store in coded form in at least one memory element that is used

for starting-up the component, and

The start-up, which initiates the appropriate actions, is repeated.

Beuten teaches:

If the activation condition is met, recognition of this fact and the desired effects it

is to have are placed in store in coded form in at least one memory element that is used

for starting-up the component (note paragraph [0014]), and

The start-up, which initiates the appropriate actions, is repeated (note paragraph

[0014]).

It would have been obvious to one of ordinary skill in the art at the time of the

invention to combine tamper resistant device of Force and the stored manipulation

detection of Beuten. It would have been obvious to one ordinary skill in the art at the

time of the invention to combine Force and Beuten because it would permit an orderly

power down of the system without any loss of data.

Conclusion

8.   The prior art made of record and not relied upon is considered pertinent to
applicant's disclosure.

        Sutherland (U.S. Patent 6,292,898) teaches an erasure of data that does not
require the use of a processor (note Abstract). When an intrusion into the secure
environment is detected, the volatile data storage device is disconnected from the
power supply and connected to a clamp which supplies current to or from a clamp
reference voltage node from or to, respectively, one or more of the designated input
nodes of the volatile data storage device to cause the magnitudes of the voltages at the
designated input nodes to become equal, thus erasing data stored in the volatile data
storage device (note column 4, lines 6-17).

        Buer (U.S. Patent 6,553,496) teaches an integrated circuit includes secure logic
that requires protection. Secure assurance logic protects the secure logic. The secure
assurance logic includes a plurality of protection modules that monitor the occurrence of
insecure conditions. Each protection module monitors a different type of insecure
condition. Each protection module asserts an alarm signal when an associated insecure
condition is detected. The alarm signals asserted by the plurality of protection modules
are stored (note Abstract).

        Giles et al. (U.S. Patent 6,968,420) teaches the storing of a tamper detection in a
flag (note column 12, line 61 through column 13, line 6).

9.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to DAVID J. PEARSON whose telephone number is (571)

272-0711. The examiner can normally be reached on Monday - Friday, 7:30am -

5:00pm; off every other Friday.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

        Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. J. P./
Examiner, Art Unit 2437

/Emmanuel L. Moise/
Supervisory Patent Examiner, Art Unit 2437